1004K-198

SPECIFICATION

Docket No. 91-C-134

TO ALL WHOM IT MAY CONCERN

BE IT KNOWN that I, Ravishankar Sundaresan am a citizen of India, residing in the State of Texas, and have invented new and useful improvements in a

METHOD OF FABRICATING A ONE-SIDED POLYSILICON THIN FILM TRANSISTOR

of which the following is a specification:

METHOD OF FABRICATING A ONE-SIDED POLYSILICON THIN FILM TRANSISTOR

1. Field of the Invention

The present invention relates generally to semiconductor integrated circuit processing, and more specifically to a method of forming a one-sided polysilicon thin film transistor.

2. Background of the Invention

The basic SRAM cell can be formed using cross-coupled CMOS inverters having 2 each n-channel and p-channel transistors. The cell is accessed by, typically, 2 n-channel control gates for a standard SRAM cell and 4 control gates for 2-port memory devices. To conserve physical layout space, the p-channel transistors are often replaced with resistive loads.

Use of the p-channel transistors as the load devices for the SRAM cell, however, results in the cell having better electrical characteristics. Such cells are faster than those using resistive loads, since the p-channel transistors provide a higher drive current than high resistance devices. Also, use of p-channel transistors gives higher immunity to soft errors, such as those caused by alpha particle impacts and noise. The primary

disadvantage of SRAM cells incorporating p-channel load transistors is that the layout area for each cell is significantly larger than those using resistive loads. This reduces device density and increases chip costs.

Bottom-gated polysilicon PMOS transistors, or an inverted form of the transistors, are often used as the p-channel transistors or load devices in the SRAM cell. Stacking the p-channel transistors over the n-channel transistors increases device density. Today, the polysilicon PMOS transistors are used, for example, as the load devices in four megabit SRAM cells to improve the stability of the cell and reduce the cell's stand-by current. These load devices, generally termed thin film transistors, may be built in 10 to 100 nanometers of polysilicon deposited on top of an oxide layer. In most applications, the gate of the thin film transistor is shielded at the bottom of the transistor body by a layer of oxide as shown in the prior art Figure 1. After the gate 50 formation, a gate oxide layer is formed over the gate thus encapsulating the gate. A thin film of polysilicon 52 is deposited covering the gate. The thin film of polysilicon is appropriately doped to form an n-channel region above the gate and p^+ source and drain regions adjacent to the n-channel region and above the gate.

The typical bottom-gated thin film transistor, however, has a high grain-junction leakage current. The presence of grain boundary traps between, for example, the p^+ drain region and the n-channel region causes field-enhanced generation current. This field enhanced current causes the leakage or off-state current of the cell to be high.

Several methods have been proposed to control the field-enhanced current in the bottom-gated polysilicon thin film transistor. See, for example, A POLYSILICON TRANSISTOR TECHNOLOGY FOR LARGE CAPACITY SRAMs, by Ikeda et al, IEDM 469-472, 1990 and A 59 um^2 SUPER LOW POWER SRAM CELL USING A NEW PHASE-SHIFT LITHOGRAPHY, by T. Yamanaka et al, IEDM 477-480, 1990. A gate to drain off-set structure of the polysilicon PMOS transistor is proposed whereby the leakage current and the stand-by dissipation power required for the memory cell are reduced to more acceptable levels.

As shown in prior art Figure 2, the heavily doped p+ drain region 54 is offset from the transistor gate 50. However, the lightly doped n-channel region which extends further over the transistor gate has the same doping concentration as the gate which results in some additional current loss. It would therefore be desirable to provide an improved off-set structure which reduces the drain electric field without compromising the drive current. It would further be desirable to form the improved structure utilizing current fabrication techniques easily adapted for use with standard integrated circuit process flows.

SUMMARY OF THE INVENTION

The invention may be incorporated into a method for forming a semiconductor device structure, and the semiconductor device structure formed thereby, by forming a first conductive structure over a portion of the integrated circuit. A first dielectric layer is formed over the first conductive structure. A polysilicon layer, having a first and a second end, is formed over the first dielectric layer. A channel region is formed in the polysilicon layer substantially over the first conductive structure. A source region is formed in the polysilicon layer adjacent to the first end of the channel region. A LDD region is formed in the polysilicon layer adjacent to the second end of the channel region. A drain region is formed in the polysilicon layer adjacent to the LDD region.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

Figure 1 illustrates the prior art bottom-gated polysilicon PMOS transistor.

Figure 2 illustrates the prior art off-set gate to drain structure of the polysilicon PMOS transistor.

Figures 3-6 are the cross-sectional views of the fabrication of a semiconductor device structure according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

Referring to **Figure 3**, an integrated circuit device is to be formed on a dielectric layer 10. A polysilicon gate electrode 12 is formed over the substrate 10. The polysilicon gate 12 is appropriately doped with a p-type dopant such as boron or an n-type dopant such as arsenic or phosphorous as known in the art. A dielectric layer 14 is formed over the integrated circuit encapsulating the gate electrode 12. Layer 14 may typically be an

oxide or an oxide/nitride composite. A substantially planar polysilicon layer 16 is then formed over the device to form the source/drain and channel regions of a transistor. This structure represents a bottom-gated transistor. The transistor is inverted from a traditional transistor structure which has a gate on top with a source/drain and channel region in the substrate. This structure represents a polysilicon PMOS thin film transistor having a gate on the bottom with the source/drain and channel regions overlying the gate in a second polysilicon layer.

The polysilicon layer 16 is appropriately doped with an n-type dopant such as phosphorous or a p-type dopant such as boron to adjust the threshold voltage to a desired value. The dopant used to adjust the threshold voltage forms the n-channel region 18 overlying the gate 12. An oxide layer is then formed over the polysilicon layer 16, patterned and etched to form a screen oxide region 20. The screen oxide 20 is formed over the region of the polysilicon layer 16 which is to remain doped with an n-type dopant forming the n-channel region 18. The screen oxide layer 20 has a thickness of between approximately 1500 to 3000 angstroms. Alternatively, the screen oxide layer may comprise an oxide/nitride stack. The purpose of the screen oxide layer 20 is to protect the n-channel region from subsequent implants. A blanket p^- implant is performed as represented by the arrows to form the lightly doped drain (LDD) p^- regions 22 on either side of the n-channel region 18.

Referring to **Figure 4**, a photoresist layer 24 is formed over the device and patterned to expose a portion of the screen oxide layer 20 and one the source region 22 in the polysilicon layer 16. A heavily doped p^+ source region 26 is formed by implantation as represented by the arrows. The dopant used to form the heavily doped source region may be boron fluoride (BF_2) to a concentration of $10^{20}/cm^3$. This p^+ source region will typically be connected to Vcc and is on top of the gate and thus does not contribute to any series resistance.

Referring to **Figure 5**, the photoresist layer 24 is removed. An oxide layer is deposited over the device. Sidewall oxide spacers 26 are then formed by an etchback of the oxide layer. A blanket p^+ implant is performed as represented by the arrows to form a heavily doped p^+ drain region 28 in polysilicon layer 16 which is off-set from the gate 12. The length of the sidewall spacers 26 will define the length of the p^- LDD region 22. The transistor leakage current will be proportional to the length of the LDD region 22. Thus, a longer p. type LDD region 22 will lower the leakage current.

Referring to **Figure 6**, the screen oxide region 20 and the sidewall spacers 26 are removed. A wet etch process may be used using the polysilicon layer 16 as an etch stop. The screen oxide no longer contributes to the topography since it is removed. Conventional planarization processes may be performed followed by contact via and metallization processes. An offset gate to drain structure is formed starting with a traditional polysilicon PMOS thin film transistor. A p^+ source/drain region and an n-

channel region are formed. In this invention, however, a p^- LDD region is formed between the n-channel and the more heavily doped p^+ drain. This structure will reduce the field enhanced junction leakage. The leakage or off-state current of the transistor will be minimized providing for more stable electrical characteristics.

As will be appreciated by those skilled in the art, the process steps described above can be used with nearly any conventional process flow. While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.